

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination 09/630,348 HSU ET AL.	
		Examiner	Art Unit	Page 1 of 1 Kandasamy Thangavelu 2123

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,311,293	10-2001	Kurshan et al.	714/37
	B	US-6,496,953	12-2002	Helland, Joseph C.	714/744
	C	US-5,465,216	11-1995	Rotem et al.	716/5
	D	US-6,115,763	09-2000	Douskey et al.	710/72
	E	US-6,484,134	11-2002	Hoskote, Yatin V.	703/14
	F	US-5,263,149	11-1993	Winlow, Thomas	703/15
	G	US-5,745,501	04-1998	Garner et al.	714/741
	H	US-6,321,186	11-2001	Yuan et al.	703/15
	I	US-6,339,837	01-2002	Li, Zhe	716/5
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Rabiei et al., "Model order reduction of large circuits using balanced truncation", IEEE 1999.
	V	Schlipf et al., "An easy approach to formal verification", IEEE 1997.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.